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126	An Overview of Artificial Neuromorphic Circuits
125	Impact of Gate engineering on Analog, RF Performance of Nanoscale Barriered TM-Heterostructure DG-MOSFET.
124	Area Efficient Energy Saving Inexact Multiplier for Error Resilient Applications
123	Investigating the Linearity Behavior of Dual Gate Junction less MOSFET with high-K Gate Stack at Cryogenic Temperatures
122	Doping-Less Underlapped Dielectric Modulating Bio-Tunnel FET Accomplishing Repulsive Steric Hindrance
121	Study on Sensitivity Parameters of Staggered Heterojunction Gate Stack Tunnel FET Biosensor
120	Thermal Effects on Performance Parameters of Gate Stack DG-MOSFET based Bio-Sensor
119	Implementation and Investigation of Quantum Characteristics of Cytosine Single â€“walled Nanotube Transistor: A DFT Based Approach
118	Analog/RF Performance Analysis of a Novel Si0.9Ge0.1/InAs Charge Plasma Based Junctionless TFET
117	A Novel Technique of Enhancing CMRR of Fully-Differential Instrumentation Amplifier Using High Gain CMFB Loop
116	A super threshold compact silicon neuron circuit for different neural dynamics suitable for spiking neural network
115	CV Analysis and Linearity Performance of InGaN Notch Dielectric Modulated Dual Channel GaN MOSHEMT for Reliable Label-free Biosensing
114	Simulation Study of Charge Plasma Nanotube FET for Low Power Mixed Signal Circuit in IoT Applications
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110	Gene Co expression analysis for identifying some regulatory genes in human lung cancer
109	Macaroni Channel-Nanowire-Field Effect Transistor (MC-NW-FET) For Gate Induced Drain Leakage (GIDL) Reduction Application
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103	A Novel 2D Mapping Scheme for Nearest Neighbor Design of Quantum Circuits
102	Impact of Trap Charge effects on the Performance of 2D material-based FET

101	MEMS-Based Piezoresistive Pressure Sensor Using Two Concentric Wheatstone Bridge Structure for Intracranial Pressure Measurement
100	Complex Odia Handwritten Character Recognition using Deep Learning Model
99	Performance Evaluation of LiNbO3-based Negative Capacitance Field Effect Transistors (NCFETs)
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72	A 0.3 V, 4th order low-pass OTA-C filter using bulk-driven technique for EEG applications
71	A Review Article on the usage of Different Materials and Different Device architectures in the Design of Tunnel Field Effect Transistor
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69	A Unified Approach for Realization of IIR Filters in Delta Domain
68	Single Event Upset Mechanism in SRAM Latch and Its Circuit-Level prevention Technique
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66	Direct wafer-bonded two terminal GaAsP/Si dual junction solar cell with 19.80% efficiency
65	Analytical model of a Dielectric-Modulated Triple Material Stacked Surrounding Gate Junctionless MOSFET-based label-free biosensor
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19	A Novel Extended Back-Gate Negative Capacitance TFET for Improved Device Performance
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17	Design of a passive beamforming circuit with -37.5 dB return loss and -42 dB isolation loss for a multibeam antenna in 5G applications
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10	Doping Induced Threshold Voltage and ION/IOFF Ratio Modulation in Surrounding Gate MOSFET for Analog Applications
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8	Comparative Analysis of Short Channel Effects in Dopingless Charge Plasma Based Nanowire FET
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6	Design and Simulation of Ultra-Low-Power Parallel Summation Logarithmic Amplifier
5	Novel Mode Changing Features in the Design of Quaternary Logic Gates using CNTFET
4	Two dimensional modeling of dual material double gate TFET in stacked hetero-dielectrics with split high-K materials
3	Selective growth of ZnO nanowires by employing voltage-assisted hydrothermal growth technique
2	The Effect of Back-Barrier on the Performance Enhancement of III-Nitride/Î²-Ga2O3 Nano-HEMT
1	Performance analysis of PLL based DSGCP (Double Stage Grid Connected Photovoltaic) system with non-linear load under normal and various grid fault conditions