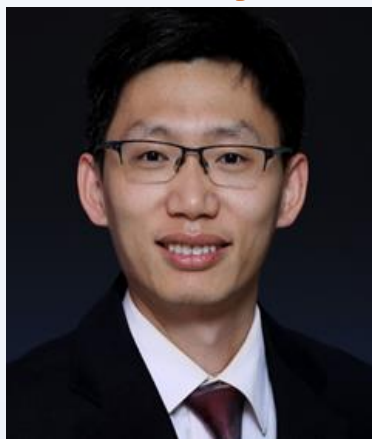*Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits and HKUST – ACE Online Seminar Series*

Design and Optimization of RRAM based Computation-in-Memory Chips

Bin GAO, Tsinghua University

6 Nov 2020
10:00-11:30 AM
VIA ZOOM
REGISTRATION:

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Recent advances in AI technology bring great challenges on the computing platform. Conventional platform based on CMOS devices and von Neumann architecture becomes more and more difficult to further improve the computing efficiency. The concept of Computation-in-Memory (CIM) based on the emerging non-volatile memory devices, such as resistive random access memory (RRAM), provide new solutions for processing data-intensive tasks with very high energy-efficiency. However, due to the intrinsic non-ideal effects of RRAM devices and circuits, up to date, the integration density and computing accuracy of the RRAM based CIM systems still cannot compete with CMOS based AI chips. This talk will first introduce the principles of RRAM based CIM technology. The performance requirements and key challenges will be discussed. Then it will talk about our recent work on multi-scale modeling of analog RRAM devices. After that, the co-design framework from device level, to circuit, architecture, and algorithm levels will be presented. This talk will also show some hardware implementations and verifications based on the guidelines of our simulation tools. Finally, I will provide some views on possible research directions in the future development on CIM applications.

Biography: Bin Gao is currently an Associate Professor with the Institute of Microelectronics, Tsinghua University, Beijing, China. He received the B.S. degree in physics from Peking University, Beijing, China, in 2008, and Ph.D. degree in Microelectronics from Peking University in 2013. In 2010, he was a Visiting Scholar with Nanyang Technological University, Singapore, and also with the Institute of Microelectronics, A*STAR, Singapore. In 2012, he was a Visiting Scholar with Stanford University, Stanford, CA, USA. In 2015, he joined Tsinghua University as an Assistant Professor, and became an Associate Professor in 2017. His current research interests include modeling, design and fabrication of emerging semiconductor devices, especially RRAM. He has published more than 100 technical papers, including 38 papers on the IEDM, ISSCC and VLSI, as well as several journal papers on Nature, Nature Electronics, Nature Communications, Proceedings of the IEEE, etc. His total citation is over 5000. He was a recipient of the IEEE EDS Master Student Fellowship in 2009, and a recipient of the IEEE EDS Ph.D. Student Fellowship in 2012. He received China Industry-University Cooperation Innovation Award with GigaDevice in 2017. He serves as MS Sub-Committee Chair of EDTM 2021, and Technical Program Committee Members of IEDM, DAC, IRPS, etc.